

SELF TESTING METHOD FOR INTEGRATED CIRCUIT DEVICE**Patent Number:** JP2000188311**Publication date:** 2000-07-04**Inventor(s):** MURAI TAKASHI; SAEKI TAKAHIRO**Applicant(s):** SHARP CORP**Requested Patent:** ☐ JP2000188311**Application Number:** JP19980365856 19981224**Priority Number(s):****IPC Classification:** H01L21/66; G01R31/28; G11C29/00; H01L27/04; H01L21/822**EC Classification:****Equivalents:****Abstract****PROBLEM TO BE SOLVED:** To shorten a wafer test time.**SOLUTION:** In order to test an integrated circuit device (chip) having a nonvolatile semiconductor storage device inside, peripheral circuits in the chip to be tested are tested by placing a test circuit 4 in operation with the electric power, generated by an ultraviolet-ray power generating device 3 in a process the ultraviolet-ray power generating device 3, and test circuit 4 are formed on the wafer 1 where chips 2 to be tested are formed and irradiation with ultraviolet rays is performed for the initialization of the nonvolatile semiconductor storage device.

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BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic diagram of a wafer 1.

FIG. 2 is a schematic diagram of a chip 2.

FIG. 3 is a schematic diagram of a test circuit 4.

FIG. 4 is a schematic diagram of a test circuit 4.

FIG. 5 is a schematic diagram of a test circuit 4.